A/Reissue

EN995137B

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Reissue Application No.:		:
Filed:	Herewith	:
Applicant:	Eric Arthur Johnson	:
Patent No.:	5,726,079	:
Issued:	March 10, 1998	:
For:	THERMALLY ENHANCED FLIP CHIP PACKAGE AND METHOD OF FORMING	:

REISSUE APPLICATION TRANSMITTAL

Assistant Commissioner for Patents
Box Reissue Application
Washington, D.C. 20231

S I R :

Reissue under 35 U.S.C. §§ 251-252 and 37 C.F.R. §§ 1.171-1.179 is requested of U.S. Patent No. 5,726,079 which issued on March 10, 1998 to Eric Arthur Johnson. That patent remains valid and enforceable.

Transmittal herewith is the application for reissue. Enclosed are the following:

1. Specification, Claims, and Drawing

(a) Six (6) pages of specification, including four (4) claims, and one (1) page of abstract.

(b) Two (2) sheets of formal drawing. No changes in the drawing upon which the original patent was issued are to be made. Therefore, pursuant to 37 C.F.R. § 1.174, please find attached a copy of the printed drawing of the patent and a drawing transfer request.

2. Declaration and Power of Attorney

Seven (7) pages of Declaration and Power of Attorney.

3. Offer of Surrender

An offer to surrender the original letters patent by the inventor in accordance with 37 C.F.R. § 1.178, along with an assent by the assignee.

4. Letters Patent

A copy of the original letters patent. Please accept a copy rather than the original letters patent for purposes of initial prosecution of the reissue application. The original letters patent will be submitted before the case is allowed.

5. Assignment

A certificate under 37 C.F.R. § 3.73(b) noting both an assignment from Eric Arthur Johnson to International Business Machines Corporation and PTO recordation of that assignment. Also enclosed are the assignment and the Notice of Recordation form issued by the PTO.

6. Title

An order for an abstract of title pursuant to 37 C.F.R. § 1.171 and authorization to charge Deposit Account No. 09-0457 (IBM Corporation) in the amount of $25.00.

7. Information Disclosure Statement

An Information Disclosure Statement, Form PTO-1449, and five (5) references.

8. Fee Calculated

Claims As Filed

	No. Filed (Original)	**No. Extra**	**Rate**	**Basic Fee ($760)**
Total:	4 (4)	0	$18	0
Independent:	1 (1)	0	$78	0
Filing Fee Calculation:				**$760**

9. Method of Payment

The Commissioner is hereby authorized to charge payment in the amount of $760.00 to Deposit Account No. 09-0457 (IBM Corporation). A duplicate copy of this sheet is enclosed.

10. Authorization to Charge Additional Fees

The Commissioner is hereby authorized to charge payment to Deposit Account No. 09-0457 (IBM Corporation) of any additional fees associated with this communication.

Respectfully Submitted,

Kevin R. Casey, Reg. No. 32,117
Attorney for Applicant

KRC/kak

Dated: August 24, 1999

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The Assistant Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **09-0457 (IBM Corp.)** of any fees associated with this communication.

EXPRESS MAIL Mailing Label Number:EL230195120US
Date of Deposit: August 24, 1999

I hereby certify that this paper and fee are being deposited, under 37 C.F.R. § 1.10 and with sufficient postage, using the "Express Mail Post Office to Addressee" service of the United States Postal Service on the date indicated above and that the deposit is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231

Kathleen C. Libby

THERMALLY ENHANCED FLIP CHIP PACKAGE AND METHOD OF FORMING

This application is a division of application [of] Ser. No. 08/666.155 filed Jun. 19. 1996. now abandoned.

BACKGROUND OF THE INVENTION

1. Technical Field

This invention relates generally to encapsulated flip chips and more particularly to a flip chip package having a thermally conductive member encapsulated with the flip chip.

2. Background Art

Flip chips are small semiconductor dies having terminations all on one side in the form of solder pads or bump contacts. Typically. the surface of the chip has been passivated or otherwise treated. The flip chip derives its name from the practice of flipping. or turning. the chip over after manufacture. prior to attaching the chip to a matching substrate.

Flip chip packages require a cover of some type over the [silicone] silicon chip to protect it and to provide a large flat surface for pick-and-place operations. However. any cover or encapsulant above the chip increases the thermal resistance path to an ambient environment and. hence. the operational temperature of the chip.

Thermally conductive caps have also been provided for flip chips. Typically. a capped chip has a thin layer of a thermally conductive grease between the chip and the cap.

However. it has been found that during thermal cycling. the grease has a tendency to be pumped. or displaced from the interface between the chip and the cap. thus increasing the thermal resistance of the interface.

The present invention is directed to overcoming the problems set forth above. It is desirable to have a flip chip package that provides low thermal resistance. and is economical to manufacture. It is also desirable to have such a flip chip package and method of manufacture that uses conventional transfer mold techniques. It is also desirable to have such a flip chip package that does not require the presence of a thermally conductive grease between the chip and a heat conducting member.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention. a flip chip package includes a substrate having a plurality of electrical circuits disposed within the substrate. a flip chip mounted on the substrate in electrical communication with predefined ones of the electrical circuits disposed in the substrate. and a thermally conductive planar member disposed in thermally conductive contact with an upper surface of the flip chip. The flip chip package also includes the substantially rigid dielectric material that surrounds the edge surfaces of the thermally conductive planar member. the edge surfaces of the flip chip. and at least a portion of the substrate.

Other features of the flip chip package embodying the present invention [includes] include the thermally conductive planar member having a thickness selected to provide a composite structure with the flip chip that extends a predetermined distance above the substrate.

In accordance with another aspect of the present invention. a method of forming a thermally enhanced flip chip package includes providing a substrate and a flip chip which are connected together such that the electrical con-

tacts on the flip chip are in electrical communication with predetermined ones of the electrical contacts on the substrate. The method also includes providing a thermally conductive planar member which is placed on the upper surface of the flip chip in thermally conductive communication with the upper surface. The assembled planar member, flip chip and substrate are placed in a mold cavity wherein a predefined portion of the substrate cooperates to form a substantially closed cavity. The moldable dielectric material is injected into the closed mold cavity and, after curing, forms a substantially rigid covering about the edges of the thermally conductive planar member, the flip chip, and the predefined portion of the substrate.

Other features of the method of forming a thermally enhanced flip chip package include selecting a thermally conductive planar member having a thickness that is selected so that when the thermally conductive planar member is placed on the flip chip, the combined thickness of the planar member and the distance that the flip chip extends above the surface of the substrate, are substantially equal to the height of the aforementioned mold cavity.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic sectional view of a flip chip package embodying the present invention, showing the flip chip and substrate components of the package in elevation; and

FIG. **2** is a flow diagram of the principal steps carried out in forming a flip chip package, in accordance with the method embodying the present invention.

DETAILED DESCRIPTION OF A PRESENTLY PREFERRED EXEMPLARY EMBODIMENT

A flip chip package **10** embodying the present invention, is shown schematically in FIG. **1**. The flip chip package **10** includes a flip chip **12** that has a plurality of electrical contacts **14** that are electronically connected, for example by soldered joints, to corresponding contacts associated with one or more electrical circuits disposed in a substrate member. The substrate member **16** is typically a laminated circuit board having a number of electrical circuits defined within the member and is adapted for interconnection with other components of an electronic assembly. The flip chip **12** has a planar upper surface [12] **18** that is spaced from the substrate **16** by a predefined distance, and a plurality of edge surfaces **20** that extend around a defined perimeter of the planar surface **18** and are disposed in substantially perpendicular relationship with the planar surface **18**.

Importantly, the thermally enhanced flip chip package **10** embodying the present invention includes a thermally conductive planar member **22** that is disposed in thermally conductive communication with the planar upper surface **18** of the flip chip **12**. The thermally conductive planar member **22** has a plurality of edge surfaces **24** that extend around the periphery of the planar member **22**.

The thermally enhanced flip chip package embodying the present invention also includes a substantially rigid dielectric material **26**, such as Toshiba XK6000 thermoset plastic, that surrounds, in intimate bonded contact, the edge surfaces **24** of the thermally conductive planar member **22**, the edge surfaces **20** of the flip chip **12**, and at least a portion of the laminated substrate **16**. The dielectric material **26** effectively encapsulates the flip chip **12**, and a portion of the planar member **22** and the substrate **16**, without covering the upper exposed surface of the thermally conductive planar member **22**.

In one embodiment of the present invention, it is desirable to form the flip chip package **10** by transfer mold techniques.

To reduce the number of molds that may be required to accommodate variously sized chips, the thermally conductive planar members **22** may be formed by stamping from sheets, in a variety of thicknesses, and at very low cost. By using the appropriate thickness of planar member **22**, various thicknesses of chips may be accommodated within a single mold. For that purpose, it is desirable that the thermally conductive planar member **22** have a thickness that is selected to provide a composite structure, when mounted on top of the flip chip **12**, that extends a fixed predetermined distance above the substrate member **16**. Thus, by simply varying the thickness of the planar member **22**, the same mold cavity may be used for variously sized chips.

In the preferred embodiment, the thermally [conducted] conductive planar member **22** is placed in the mold cavity prior to inserting the flip chip **12** attached to the substrate member **16** into the mold cavity, after which the dielectric material **26** is injected into the cavity. Alternatively, the thermally conductive planar member **22** may be prebonded to the planar upper surface **18** of the flip chip **12** by a thermally conductive adhesive material **28** prior to placing the bonded assembly into the mold cavity and injecting the dielectric material **26** into the cavity.

Preferably, the thermally conductive planar material is formed of copper, which has a thermal coefficient of expansion substantially equal to that of laminated glass-epoxy printed wiring boards.

The method of forming an enhanced flip chip package **10** embodying the present invention includes providing a substrate member **16** having a plurality of electrical contacts disposed on an upper surface of the substrate member, as indicated at block **30** in FIG. **2**, and also providing a flip chip **12** having a plurality of electrical contacts **14** disposed on a lower surface, as indicated at block **32**. The flip chip **12** is attached to the substrate member **16**, as indicated at block **34**, typically by a heating cycle in which solder interconnections are formed. If desired, an underfill material such as Dexter's HYSOL™ 4511 epoxy may be used to provide electrical isolation between the connected contacts.

A thermally conductive planar member **22**, preferably a copper plate, is provided as indicated at block **36**, and then placed on the upper surface **18** of the flip chip **12** so that the planar member **22** is in thermal communication with the upper surface of the flip chip **12**, as indicated at block **38**, either by intimate contact or by an adhesive bond to the upper surface **18**.

The aligned thermally conductive planar member **22**, the flip chip **12**, and the substrate member **16** are then placed in a mold cavity, as indicated at block **40**. A portion of the substrate member **16**, i.e., the immediate area surrounding the mounted flip chip **12**, cooperates with other predefined surfaces of the mold cavity to form a substantially closed cavity. A moldable dielectric material, such as a highly-filled epoxy, is then injected into the transfer mold, as indicated at block **42**, and surrounds the edge surfaces **24** of the planar member **22** and the flip chip **12**. As can be seen in FIG. **1**, the dielectric material **26** also is forced into intimate contact against a portion of a lower surface of the thermally conductive member **22** and the surrounding area of the surface of the substrate member **16**, thus essentially providing effective encapsulation of the flip chip **12** and the thermally conductive planar member **22** with the substrate member **16**.

After curing the moldable dielectric material [**28**] **26**, as indicated at block **44**, a substantially rigid dielectric covering is thereby formed over the thermally conductive planar member **22**, the flip chip **12**, and the predefined portion of the

substrate member **16**, providing an integral, essentially inseparable, package **10**. After curing, the formed package **10** is removed from the mold, as indicated at block **46**.

Preferably, in carrying out the method of forming a thermally integrated flip chip package **10**, a single mold cavity may be advantageously used for a variety of differently sized flip chips **12** by varying the thickness of the planar member **22**. If accurately sized, there will be no dielectric material over the top exposed surface of the planar member **22**. This is desirable so that the heat conductive path from the flip chip **12** has a minimum number of interfacial resistances in the path of heat flow. Thus, it is desirable to control the thickness of the planar member **22** so that its upper surface is flush with the surface of the mold compound on the finished part. In this arrangement, no adhesive material would be required between the thermally conductive planar member **22** and the flip chip **12**, although a thermally conductive adhesive material [as] may be used, if desired, as an assembly aid.

In summary, the flip chip package arrangement and method of forming provides a flip chip package **10** that is reliable in performance and easy to manufacture. These objectives are accomplished by using the transfer mold technique to encapsulate the chip, along with a thermally conductive planar member **22** that is used as an insert during molding. Alternatively, the insert **22** [maybe] may be attached to the top of the flip chip **12** by use of a small amount of a thermally conductive adhesive material.

The planar member **22** may be stamped from sheets, of varying thicknesses, at very low cost. By using the appropriate thickness of insert, any thickness chip can be accommodated within a single mold. The thickness of the planar member **22** should be selected to match the height of the cavity in the mold, when combined with the flip chip **12**, to avoid excessive loads on the chip-to-substrate interconnection when the mold is clamped.

The thermal performance of a flip chip package **10** embodying the present invention, preferably without an adhesive layer, will be substantially identical to that of a capped chip, using thermal grease. Furthermore, the flip chip package **10** embodying the present invention has the advantage of avoiding any possibility of pumping which may deplete the grease layer and increase the thermal resistance, as may occur with capped chips. Importantly, the performance of the flip chip package **10** embodying the present invention, is significantly better than that of any package which uses overmold without the thermally conductive planar member **22**. In addition, bending of the package **10** is reduced as a result of balancing the expansion of the substrate member **16** and the planar member **22**, providing high reliability and improved coplanarity when embodied in a Ball Grid Array (BGA) package.

Although the present invention is described in terms of a preferred exemplary embodiment, those skilled in the art will recognize that changes in the order in which various components, e.g., the substrate member **16**, the thermally conductive planar member **22**, and the flip chip **12**, are provided may be [varied] made without departing from the spirit of the invention. Such changes are intended to fall within the scope of the following claims. Other aspects, features, and advantages of the present invention may be obtained from a study of this disclosure and the drawings, along with the appended claims.

What is claimed is:

1. A method of forming a flip chip package, comprising:

providing a substrate member having a plurality of electrical contacts disposed thereon;

providing a flip chip having a plurality of electrical contacts disposed on a lower surface, a planar upper surface, and a plurality of edge surfaces extending between said lower and said upper surfaces;

connecting the electrical contacts of said flip chip with selected ones of the electrical contacts on said substrate;

providing a thermally conductive planar member having a plurality of peripherally disposed edge surfaces;

[placing said thermally conductive planar member in thermally conductive communication with said upper surface of the flip chip;]

placing said thermally conductive planar member, said flip chip, and said substrate member in a mold cavity wherein a predefined portion of said substrate member cooperates with said mold cavity to define a sealable cavity;

injecting a moldable dielectric material into said sealable cavity;

curing said moldable dielectric material and thereby forming a sealed rigid dielectric covering about the edge surfaces of said thermally conductive planar member.

the edge surfaces of said flip chip, and said predefined portion of said substrate member and forming an encapsulated flip chip package comprising said thermally conductive planar member, said flip chip, and said [predefined portion of said] substrate member; and

removing said flip chip package from said [sealed cover-][ing] mold cavity.

2. A method of forming a flip chip package, as set forth in claim [1] 4, wherein said mold cavity has a first selected height and said thermally conductive planar member has a thickness selected so that when mounted on the upper planar surface of the flip chip, said planar member extends a second selected height above said substrate member, said second selected height being substantially equal to the first selected height of said mold cavity.

3. A method of forming a flip chip package, as set forth in claim [1] 4, wherein placing said thermally conductive planar member [on] in thermally conductive communication with said upper surface of the flip chip includes bonding said planar member to the upper surface of the flip chip with a thermally conductive adhesive material.

4. A method of forming a flip chip package, as set forth in claim 1, further comprising the step, after providing a thermally conductive planar member, of placing said thermally conductive planar member in thermally conductive communication with said upper surface of the flip chip.

* * * * *

ABSTRACT

A thermally conductive planar member is in thermally conductive communication with a flip chip encapsulated within a dielectric material that surrounds portions of the thermally conductive planar member, the flip-chip, and a predefined portion of a substrate member. The present invention provides a flip chip package having pick-and-place capability without the thermal resistance disadvantage of capped chip packages.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant:	Eric Arthur Johnson	:
Patent No.:	5,726,079	:
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For:	THERMALLY ENHANCED FLIP CHIP PACKAGE AND METHOD OF FORMING	:

DECLARATION AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Box Reissue Application
Washington, D.C. 20231

S I R :

The undersigned applicant, Eric Arthur Johnson, hereby declares that he is a citizen of the United States and resides at 7 Jeffrey Heights, Greene, New York 13778, U.S.A.; that he is an employee of the assignee (International Business Machines Corporation) of the subject U.S. Patent No. 5,726,079; that he believes himself to be the original, first, and only inventor of the invention described and claimed in U.S. Patent No. 5,726,079 and for which invention he solicits a reissue patent; that he does not know and does not believe that the invention was ever known or used in the United States before his invention thereof; that he has reviewed and understands the contents of U.S. Patent No. 5,726,079, including the claims; and that he believes the original patent to be defective or partly inoperative because (a) the claims include elements or limitations lacking antecedent basis and causing inconsistencies, rendering the claims potentially ambiguous; and (b) he claimed less than he had a right to claim in the original patent in one respect.

I. Amendments to Claim 1

A. *Limitations Lacking Antecedent Basis And Having Inconsistencies*

Specifically, upon review with his patent attorney, Mr. Lawrence R. Fraley, Esq., corporate patent counsel at International Business Machines Corporation, of the issued U.S. Patent No. 5,726,079 on or about August 1, 1998, the applicant determined that method claims 1 and 3 of the issued patent recite limitations lacking antecedent basis and having inconsistencies, rendering the claims potentially ambiguous. Mr. Fraley subsequently conferred with outside patent attorney, Mr. Kevin R. Casey, Esq. of Ratner & Prestia, Suite 301, One Westlakes, Berwyn, Valley Forge, PA 19482.

The '079 patent issued based on U.S. Patent Application Serial No. 08/715,212 filed on September 17, 1996 as a division of U.S. Patent Application Serial No. 08/666,155 filed on June 19, 1996 (now abandoned). Mr. Casey was working with Mr. Fraley on prosecution of U.S. Patent Application Serial No. 08/842,417 filed on April 24, 1997. The '417 application is a division of the '212 application from which the '079 patent issued. Mr. Fraley's work with Mr. Casey on prosecution of the related '417 application prompted, in part, his review of the claims of the '079 patent. The references listed on the Information Disclosure Statement submitted herewith were made of record during prosecution of the '417 application.

In reviewing the claims of U.S. Patent No. 5,726,079, it was determined that the last limitation of claim 1 incorrectly recites a "sealed covering." The step of the method which includes that limitation recites "removing said flip chip package from said sealed covering." The flip chip package (10) includes a thermally conductive planar member (22), a flip chip (12), and a substrate member (16). A sealed rigid dielectric covering (26) is formed about the edge surfaces of the thermally conductive planar member, the edge surfaces of the flip chip, and a predefined portion of the substrate member.

As the specification and prosecution history show, the package (10) is not removed from the sealed covering (26). The specification, at column 4, lines 2-3, states that removal of the package (10) is from the mold. Originally filed claim 5 (issued following prosecution as claim 1) recited removal from "said closed cavity." Accordingly, claim 1 has been revised to correctly recite that removal of the flip chip package is from the "mold cavity."

Another limitation in claim 1 recites that the "encapsulated flip chip package" comprises "said thermally conductive planar member, said flip chip, and said predefined portion of said substrate member." (Emphasis added.) In fact, the package includes more than the predefined portion of the substrate member; the package includes the entire substrate member. *See* specification at column 2, lines 33-54. Accordingly, submitted in the reissue application is an amended independent claim 1. Claim 1 does not recite the unnecessary limitation directed to "said predefined portion of" the substrate member.

B. *Broadening Limitation*

Upon further review with his patent attorney, the applicant also determined that the method disclosed in the patent, for forming a flip chip package, had not been subjected to the breadth of patent protection to which the applicant is entitled. As one object of his invention, the applicant states: "It is desirable to have a flip chip package that . . . is economical to manufacture." *See* specification at page 2, lines 7-9. To achieve that object, one of the concepts disclosed in the specification of the '079 patent is a method in which:

> The assembled planar member, flip chip and substrate are placed in a mold cavity wherein a predefined portion of the substrate cooperates to form a substantially closed cavity. The moldable dielectric material is injected into the closed mold cavity and, after curing, forms a substantially rigid covering about the edges of the thermally conductive planar member, the flip chip, and the predefined portion of the substrate.

See specification from page 3, line 31 to page 4, line 7. For additional details, see specification on page 9, lines 1-16. The steps of the method outlined above are all recited in claim 1.

Claim 1 also recites, however, the step of "placing said thermally conductive planar member in thermally conductive communication with said upper surface of the flip chip." Although the '079 patent teaches that step, the step is unnecessary to practice the invention. In reviewing the coverage provided by the claims of the '079 patent, for the method discussed above, it was determined that claim 1 was inadvertently drafted in excessively narrow terms and, therefore, does not encompass all that the applicant had a right to claim. Claim 1 is the broadest claim; that claim includes a limitation which is not believed necessary to practice the invention. In particular, claim 1 recites an additional step.

Accordingly, submitted in the reissue application is an amended independent claim 1. Claim 1 does not recite the unnecessary limitation to "placing said thermally conductive planar member in thermally conductive communication with said upper surface of the flip chip." Rather, the limitation has been deleted from claim 1 and included in a new, dependent claim 4. The amendment to claim 1 has required minor amendments to claims 2 and 3 so that each of those claims now depend from claim 4.

II. Amendment to Claim 3

Dependent through claim 4 upon independent claim 1, claim 3 specifies that the step of placing the thermally conductive planar member "on" the upper surface of the flip chip includes bonding the planar member to the upper surface of the flip chip with a thermally conductive adhesive material. The limitation directed to placement "on" the upper surface lacks an antecedent basis. Claim 4 recites that the thermally conductive planar member is placed "in thermally conductive communication with" the upper surface of the flip chip. Therefore, claim 3 has been amended to recite that the step of placing the thermally conductive planar member "in thermally conductive communication with" the upper surface of the flip chip includes

bonding the planar member to the upper surface of the flip chip with a thermally conductive adhesive material.

III. Amendments to the Specification

Upon re-reading the '079 patent, a number of typographical and idomatic errors were discovered in the specification. Accordingly, the specification has been amended to correct these errors. Although no substantive changes have been made, the amended specification is submitted to conform this case to the formal requirements and long-established formal standards of U.S. Patent and Trademark Office practice, and to provide improved idiom and better grammatical form.

IV. Conclusion

Thus, submitted herewith are amended claims 1-3 and new claim 4. The two limitations of claim 1 causing inconsistencies and rendering the claim potentially ambiguous have been deleted from ("predefined portion of said") or revised in ("sealed covering" revised to "mold cavity") the original claim. The unnecessarily narrowing limitation to "placing said thermally conductive planar member in thermally conductive communication with said upper surface of the flip chip" has been deleted from claim 1 and included in claim 4. Claims 2 and 3 have been amended so that each of those claims now depend from claim 4. The limitation lacking an antecedent basis in claim 3 has been revised to recite a limitation ("in thermally conductive communication with") having an antecedent basis in claim 4.

The reissuable errors in U.S. Patent No. 5,726,079 discussed above, which render that patent partly defective or inoperative, arose without any deceptive intent.

The undersigned hereby appoints Paul F. Prestia, Reg. No. 23,031; Allan Ratner, Reg. No. 19,717; Andrew L. Ney, Reg. No. 20,300; Kenneth N. Nigon, Reg. No. 31,549; Kevin R. Casey, Reg. No. 32,117;

Benjamin E. Leace, Reg. No. 33,412; Lawrence E. Ashery, Reg. No. 34,515; James C. Simmons, Reg. No. 24,842; Robert L. Andersen, Reg. No. 25,771; Christopher R. Lewis, Reg. No. 36,201; Daniel N. Calder, Reg. No. 27,424; Louis W. Beardell, Jr., Reg. No. 40,506; Jacques L. Etkowicz, Reg. No. 41,738; Eric L. Dichter, Reg. No. 41,708; Mark J. Marcelli, Reg. No. 36,593; Christopher J. Dervishian, Reg. No. 42,480; Joshua L. Cohen, Reg. No. 38,040; Jack J. Jankovitz, Reg. No. 42,690; David L. Adour, Reg. No. 29,604; Lawrence R. Fraley, Reg. No. 26,885; John R. Pivnichny, Reg. No. 43,001; Arthur J. Samodovitz, Reg. No. 31,297; William H. Steinberg, Reg. No. 28,540; Christopher A. Hughes, Reg. No. 26,914; Edward A. Pennington, Reg. No. 32,588; John E. Hoel, Reg. No. 26,279; and Joseph C. Redmond, Jr., Reg. No. 18,753, the address of each of whom is Ratner & Prestia, Suite 301, One Westlakes, Berwyn, P.O. Box 980, Valley Forge, Pennsylvania 19482-0980 as his attorneys and/or agents to prosecute the application, and to transact all business in the U.S. Patent and Trademark Office connected with the application.

The undersigned applicant hereby acknowledges the duty to disclose information which is material to the examination of the application in accordance with 37 C.F.R. § 1.56.

Please send correspondence to:

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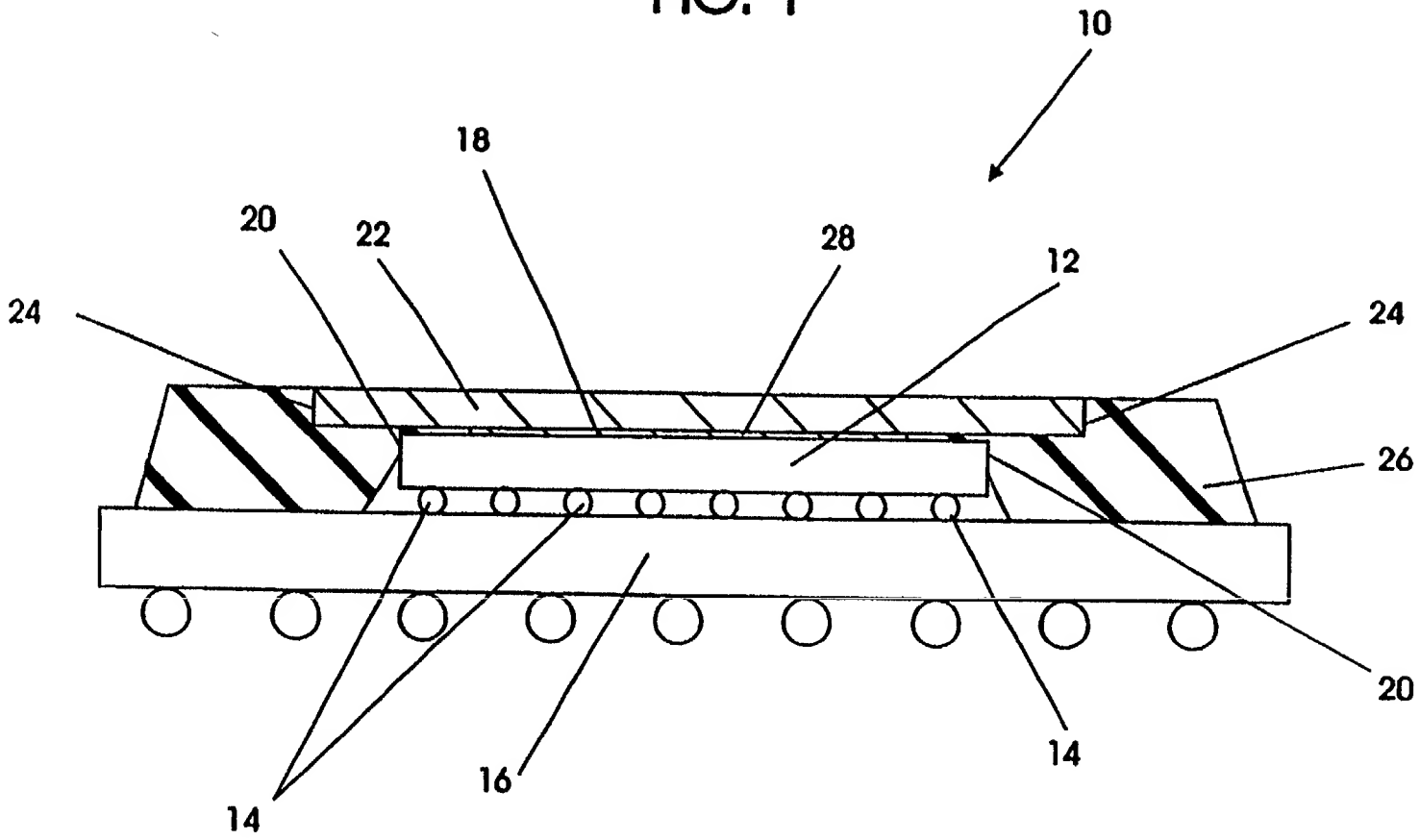
Valley Forge, PA 19482-0980

The undersigned applicant declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and

the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Dated: Aug. 16, 1999 By: Eric Arthur Johnson
Eric Arthur Johnson

FIG. 1



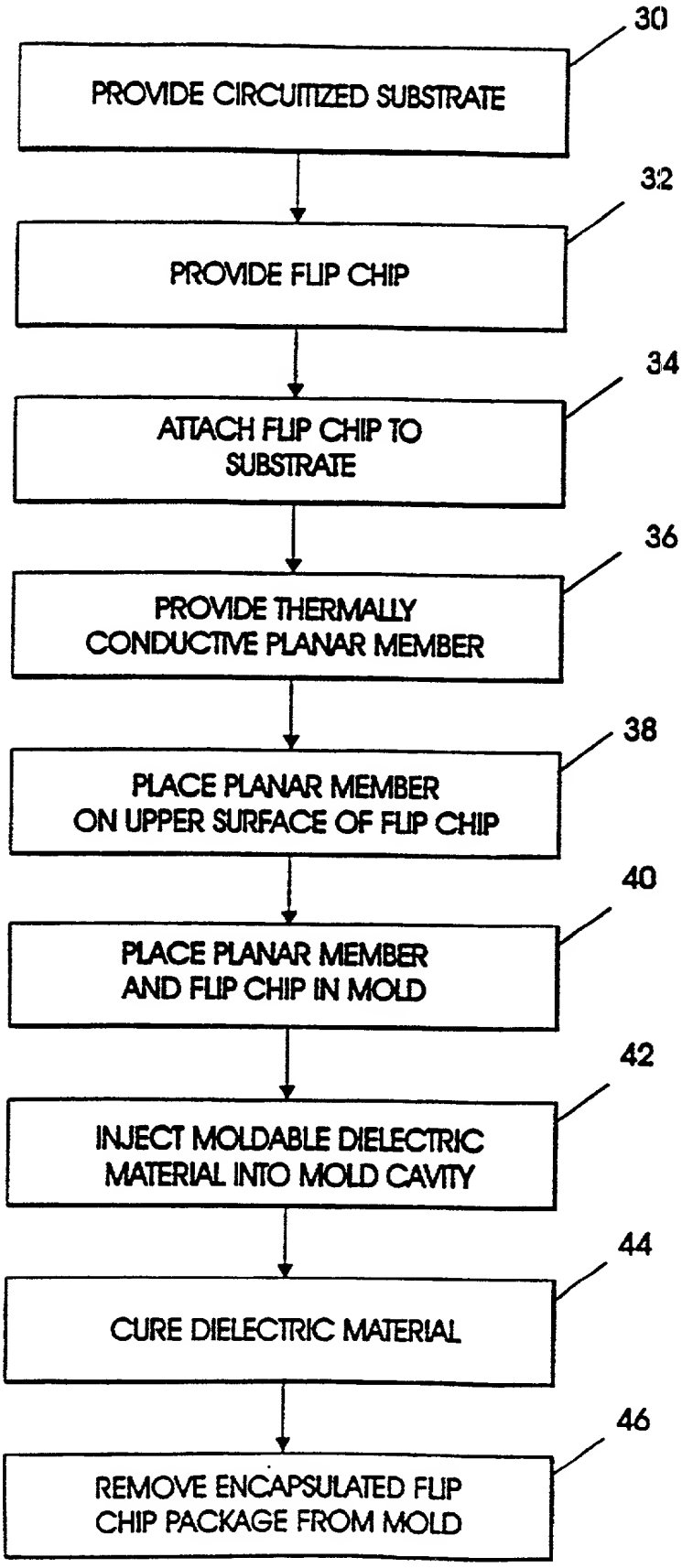

30
PROVIDE CIRCUITIZED SUBSTRATE
32
PROVIDE FLIP CHIP
34
ATTACH FLIP CHIP TO SUBSTRATE
36
PROVIDE THERMALLY CONDUCTIVE PLANAR MEMBER
38
PLACE PLANAR MEMBER ON UPPER SURFACE OF FLIP CHIP
40
PLACE PLANAR MEMBER AND FLIP CHIP IN MOLD
42
INJECT MOLDABLE DIELECTRIC MATERIAL INTO MOLD CAVITY
44
CURE DIELECTRIC MATERIAL
46
REMOVE ENCAPSULATED FLIP CHIP PACKAGE FROM MOLD

FIG. 2